Optical and Quantum Electronics (2019) 51:360
https://doi.org/10.1007/s11082-019-2079-2

# Determination of electrical parameters of ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag heterojunction diodes in dark and illumination conditions

**Serap Yiğit Gezgin**[1] · **Hamdi Şükür Kiliç**[1,2,3]

Received: 17 June 2019 / Accepted: 16 October 2019 / Published online: 24 October 2019


**Abstract**
In this work, ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag heterojunction diodes has been produced, CdS and CZTS thin film layers of the diode have been produced on ITO glass at room temperature using PLD technique. It has been produced CZTS thin films that have a polycrystalline structure that were annealed at the sulfurization temperatures of 325 °C, 350 °C and 375 °C when as-grown CZTS thin film has the amorphous structure. CdS thin films have been grown on substrate at room temperature in 15, 20 and 25 min that have polycrystalline structures. Then, CdS thin film deposited for 20 min was annealed at 200 °C temperature and, has better crystal structure compared to other thin films. Diodes have been composed of CZTS thin film annealed in 375 °C, CdS thin film was grown during 20 min and, then annealed at 200 °C temperature. According to J–V characteristics of diode, diodes exhibit some rectification behaviour in dark and show a photo-electric property under illumination conditions. In this article, the ideality factors of diodes in dark condition have been calculated, their electrical parameters of $J_{sc}$, $V_{oc}$, FF and η under the illumination condition have been determined and these electrical properties have been discussed in details.

**Keywords** Diode · CZTS · CdS · PLD · Ideality factor · Efficiency

## 1 Introduction

Cu2ZnSnS4 (CZTS) is a chalcogenide material, among the second-generation solar cells, and a p-type semiconductor in polycrystalline structure with high absorption coefficient in $10^4$ $cm^{-1}$ (Chtouki et al. 2017) and the direct band gap in 1.5 eV (Dhakal et al. 2014).

✉ Hamdi Şükür Kiliç
hamdisukurkilic@selcuk.edu.tr

[1] Department of Physics, Faculty of Science, University of Selçuk, 42031 Selçuklu, Konya, Turkey

[2] Directorate of High Technology Research and Application Center, University of Selçuk, 42031 Selçuklu, Konya, Turkey

[3] Directorate of Laser Induced Proton Therapy Application and Research Center, University of Selçuk, 42031 Selçuklu, Konya, Turkey

Materials such as Copper Indium Gallium Sulphide (CIGS), Copper Indium Sulphide (CIS) and Cadmium Tellur (CdTe) (Song et al. 2014), used as active layers, are composed of costly elements (Ga, Te, In) and toxic (Cd), but CZTS structure is made of relatively cheaper and nontoxic elements compared to these materials.

CdS semiconductors are generally used as a buffer layer to CZTS thin film solar cells. CdS is a n-type semiconductor with high photo-conductivity, a wide band gap in 2.4 eV and low electrical resistance (Moualkia et al. 2009). CdS thin film should be neither too thick to transmit photons to the absorber layer nor too thin to cause shorting due to pinholes in thin film (Moualkia et al. 2009). That is, CdS should be of appropriate thickness as a buffer layer to exhibit quantified optical, morphological and electrical properties to form an ideal p–n junction with CZTS.

CZTS and CdS thin films can be produced by techniques such as spin coating, chemical bath deposition, pulse laser deposition (PLD), magnetron sputtering (Acharya et al. 2007; Hop et al. 2008; Song et al. 2014). In this study, both CZTS and CdS thin films have been produced by PLD technique. PLD is a very useful and simple technique with tunable parameters such as laser energy, laser wavelength, laser repetition rate, ambient gas pressure, substrate temperature and target-substrate distance (Moholkar et al. 2011a, b). By setting these parameters at appropriate values, stoichiometric, epitaxial and crystalline thin films can be grown on substrate at low temperature. So, elements forming target material can be simultaneously ablated in the volume of single puls producing and high kinetic energy atoms ablated nucleate in right crystal regions on substrate and grow in a proper orientation (Cazzaniga et al. 2016; Dikovska et al. 2005; Ghimbeu et al. 2012). According to studies reported in the literature, both active and buffer layers within CdS/CdTe solar cells have been produced by PLD (Al-Mebir et al. 2016; Li et al. 2012). The pressure of background ambient gas is used during deposition of CdS thin film to prevent CdS entry into CdTe active layer. In this study, in order to prevent both the entry of the ablated CdS particle into CZTS thin films and the ablated CZTS particles on CdS thin films, the background gas pressure was not used during deposition of CdS and CZTS thin films, but target-substrate distance was increased (for CdS deposition) and laser pulse energy was kept low for ablation of both materials.

In this work, ITO/CZTS/CdS/Ag (CZTS-I), ITO/CdS/CZTS/Ag (CZTS-II) and ITO/CZTS/CdS(annealed)/Ag (CZTS-III) diode structures, in which CdS and CZTS layers were grown on substrate layer at room temperature by PLD technique. CZTS thin film has been annealed at a sulfurization temperature of 375 °C in all diode structures and CdS thin film has been annealed at 200 °C temperature in CZTS-III diode. J–V characteristics of diodes were obtained in dark and illumination conditions. It has been observed that diodes exhibited rectification behaviour in dark and photo-electric behaviour in illumination condition. Open circuit voltage ($V_{oc}$), short circuit current density ($J_{sc}$), fill factor (FF), power conversion efficiency (η) values for diodes were calculated from J–V plots.

In this study, we have noticed that the light diffuses from ITO layer to CZTS absorber and CdS buffer layers in ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag diode structures, respectively. $J_{sc}$, $V_{oc}$, FF and thus η values have changed depending on CZTS and CdS thin film layers on which the light comes upon themselves. Particularly, when the light came directly onto the buffer layer as in bifacial solar cells, more photo excited electron carriers (Jun et al. 2013; Shaafi et al. 2019) were formed in the active layer and near the depletion site and the diode' $J_{sc}$, FF and n parameters increased. (Bouchama and Ali-Saoucha 2017; Espindola-Rodriguez et al. 2017; Ge et al. 2014; Kim et al. 2016; Myny et al. 2016). Therefore, we think that ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag diodes can act as diode structures in bifacial solar cells and their performance can more enhancement if the

light comes on either side of the diodes. Furthermore, the morphology and crystal structure of CdS thin film were improved by annealing at 200 °C temperature and ITO/CdS/CZTS/Ag diode's $V_{oc}$, FF ve η values increased significantly. From this perspective, the electrical parameters given by diodes in light and dark conditions have been examined in detail in this present article.

## 2 Experimental

### 2.1 The growth of CZTS and CdS thin films by PLD

In this study, CdS and CZTS layers in ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag diode structures have been deposited on ITO coated glass (in the form of CZTS/CdS and CdS/CZTS) by using PLD technique in connection with a laser system which delivers laser beam at fundamental wavelength at 1064 nm of an Nd:YAG laser at a repetition of 10 Hz and pulse width of 5 ns. The laser beam in pulsed mode was first reflected by the mirror and then focused onto target material with a convex lens as seen Fig. 1. The vacuum chamber was evacuated down to $8 \times 10^{-6}$ mbar background pressure to form a clean environment.

Preliminary studies have been executed for a diagnostic work on CZTS and CdS thin films before production of diodes. These studies are as follows: In order to produce CZTS thin films, target-substrate distance was set to 45 mm, CZTS (Cu:Zn:Sn:S element ratio;

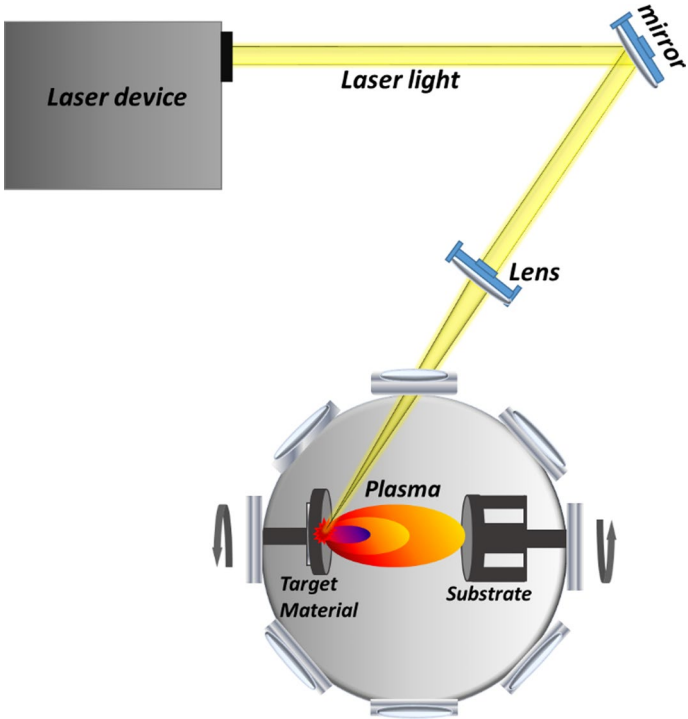


**Fig. 1** A image of PLD system and plasma formed by ablation of materials from target material

2:1:1:4 at%) target for sputtering application with 99.99% purity (purchased from Good-Will-Chine commercial company, www.chine-goodwill.com) was ablated using laser pulses with energy of 20 mJ per pulse and its thin film was produced on a microscopic glass at room temperature within 90 min. Thin films were annealed by placing next to 50 mg of sulphur powder for 30 s at each of 325 °C, 350 °C and 375 °C temperatures. To produce CdS thin film, target-substrate distance was set to 85 mm, CdS sputtering material with 99.99% purity (purchased from GoodWill-Chine commercial company, www.chine-goodwill.com) was ablated using laser pulse with 10 mJ pulse energy and its thin film were grown on a microscopic glass at room temperatures for 15, 20 and 25 min. CdS thin film deposited in 20 min that was annealed at 200 °C for 30 min in tube furnace. Afterwards, the morphologic, crystal and optical properties of CZTS and CdS thin films were examined. It has been identified that both CdS and CZTS thin films have been formed at good-qualities.

ITO/CZST/CdS/Ag and ITO/CdS/CZTS/Ag diode structures were produced on ITO coated glass and CdS and CZTS layers were also deposited by courtesy of PLD technique. CZTS thin film has been deposited on ITO coating glass (and on CdS thin film) at room temperature with experimental parameters described above. Afterwards, CZTS thin film was annealed at 375 °C sulphurization temperature. CdS thin film was grown also on ITO coated glass (and on CZTS thin film) at room temperature by a deposition process for 20 min with experimental parameters expressed in the preliminary studies. In addition, CdS thin film deposited on ITO that was annealed at 200 °C temperature. Ag contacts was deposited on ITO/CZTS/CdS, ITO/CdS/CZTS and ITO/CdS(annealed)/CZTS structures by Physical Vapour Deposition (PVD) technique. For Ag contact production, the vacuum chamber was evacuated down to about $1 \times 10^{-6}$ mbar. The deposition rate of Ag metal contacts was gradually increased from 0.1 to 0.5 Å/s. Ag thin film contacts was produced in thickness of 100 nm and an active area of 0.02 $cm^2$. The structures of ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag diode produced are demonstrated in Fig. 2a, b, respectively.

## 2.2 Material characterization

Crystalline structures, optical properties, morphology, elemental ratios of CdS and CZTS thin films in produced diodes were analysed by X-ray Powder Diffraction (XRD), UVvis spectra, Atomic force microscope (AFM) and Scanning electron microscope (SEM) and Energy-dispersive X-ray spectroscopy (SEM–EDX), respectively. The electrical parameters

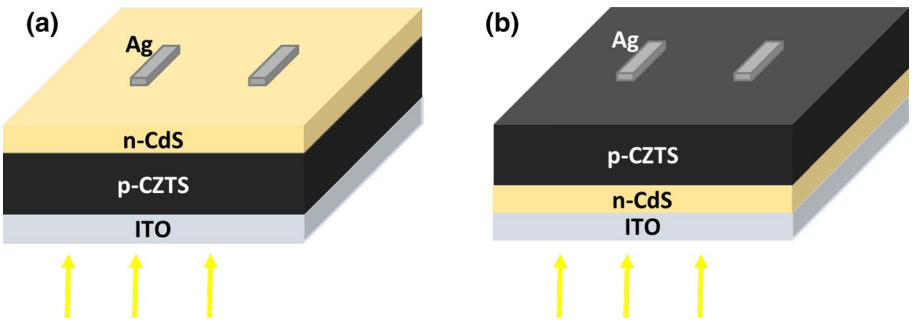


**Fig. 2** **a** Designs of ITO/CZTS/CdS/Ag and **b** ITO/CdS/CZTS/Ag diode structures generated by PLD are shown

of CZTS-I, CZTS-II and CZTS-III diode structures have been determined by J–V characterization in the dark and illumination conditions.

## 3 Discussion

### 3.1 XRD analysis

XRD spectra of CZTS**1** thin film (as-grown) grown on substrate at room temperature and CZTS(**2, 3, 4**) thin films annealed at 325 °C, 350 °C and 375 °C, respectively, are presented in Fig. 3. It was observed that all of CZTS (**2, 3, 4**) thin films annealed were grown in polycrystalline structure and have peaks in (112), (200), 220 and (312) orientations appeared at 2θ = 28°, 33°, 47° and 56° while as-grown CZTS**1** thin film has amorphous structure. CZTS**4** thin film annealed at high temperature has a main peak at (112) orientation which has the highest intensity when CZTS**2** thin film annealed at low temperature has main peak in the lowest intensity.

The size of main grain in CZTS thin films is calculated by Scherrer formula:

$$D = 0.94\lambda/\beta\cos\theta \tag{1}$$

D is main size of grain composing thin film, $\beta$ is the full-width at half-maximum of diffraction main peak, λ is the X-ray wavelength, $\theta$ is the Bragg diffraction angle in degree (Jamal et al. 2014; Khandelwal et al. 2009). The main grain sizes of CZTS**2**, CZTS**3** and CZTS**4** thin films were found to be 21.05 nm, 27.19 nm and 50.11 nm, respectively. While the annealing temperature increased, the grain size of CZTS thin films was increased and the crystal structures was developed. Also, as the kinetic energy and surface mobility of CZTS atoms at high temperature increases, the atoms tend to occupy more stable regions. Thus, existing defects in CZTS thin film begin to decrease and the crystal structure of CZTS thin film improves. Furthermore, the crystal peak of CZTS**4** thin film has higher intensity since its grain size increases as temperature increases (Khalate et al. 2017; Kim and Hong 2017). So, when CZTS thin film crystallizes better, the large grain reduce

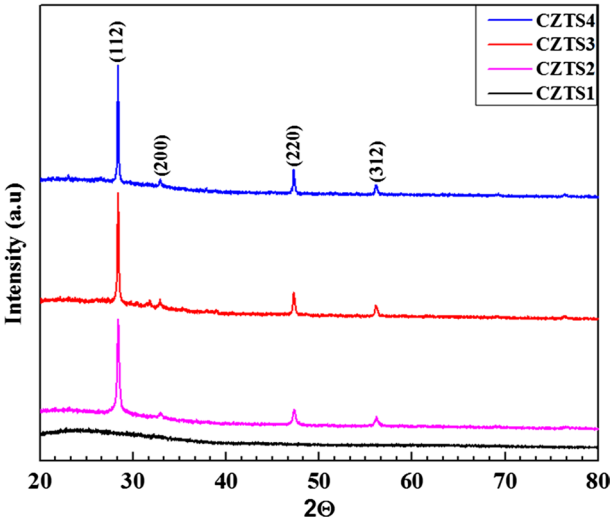


**Fig. 3** XRD pattern of as-grown CZTS**1** thin film and CZTS(**2, 3** and **4**) thin films annealed at sulfurization temperature in 325 °C, 350 °C and 375 °C, respectively

the number of grain boundaries which destroy traps that acts as recombination points of holes and electrons within the grain boundaries as well as increase the lifetime of minority charge carriers in CZTS thin film (Gaury and Haney 2016; Li and Clemens 2014; Muhunthan et al. 2015; Tang et al. 2013). Therefore, larger grains in size enables the transition of charges to side of depletion region and the charge collection in the edge of depletion region (Gaury and Haney 2016; Gupta and Tyagi 2004). In this respect, CZTS**4** thin film among four thin films produced has the highest crystal peak density which is the most ideal one in the crystal structure to use in p-n hetero junction diode structures.

Figure 4 shows XRD patterns of CdS**1**, CdS**2** and CdS**3** thin films grown on a substrate at room temperature for 15, 20 and 25 min (non-annealed), respectively and CdS**4** thin film was deposited for 20 min and annealed at 200 °C temperature. CdS thin films have polycrystalline structures with peaks at 100, 002, 101, 110 orientations. The thicknesses of CdS**1**, CdS**2** are CdS**3** are 50 nm, 70 nm and 150 nm, respectively. CdS**1** thin film at 50 nm thickness is actually in thickness of buffer layers for use in solar cells to transmit photons (Dalapati et al. 2017; Yan et al. 2018) but, has a poor crystal structure. The poor crystal structure of CdS**1** thin film can be attributed to the fact that CdS**1** deposited in a short time (for 15 min) is formed from relatively smaller grains and cannot occur in a compact structure (Tanushevski and Osmani 2018). The small grain size limits the conductivity of CdS**1** thin film and the movement of charge carriers within CdS**1** thin film (Zahra 2013), which reduces the efficiency of diodes. The crystal structure of CdS**2** and CdS**3** thin films are similar to each other and exhibit a common main peak at a direction of (002) with high intensity. But, as CdS**2** thin film is thinner, it is advantageous more than CdS**3** thin film for use as a buffer layer. Therefore, annealing of CdS**2** thin film at 200 °C temperature was found to be suitable. CdS**4** thin film obtained by annealing at 200 °C has the most intense and was developed main crystal peak. The CdS**4** thin film obtained by annealing at 200 °C temperature has the most intense and developed main crystal peaks. At high temperature, the kinetic energies of CdS atoms increase and thus they diffuse into each other and to the surrounding adatoms, resulting in larger nucleation and grain expansion. In addition, CdS**4** atoms in high kinetic energies occupying more stable regions and inactivate defects

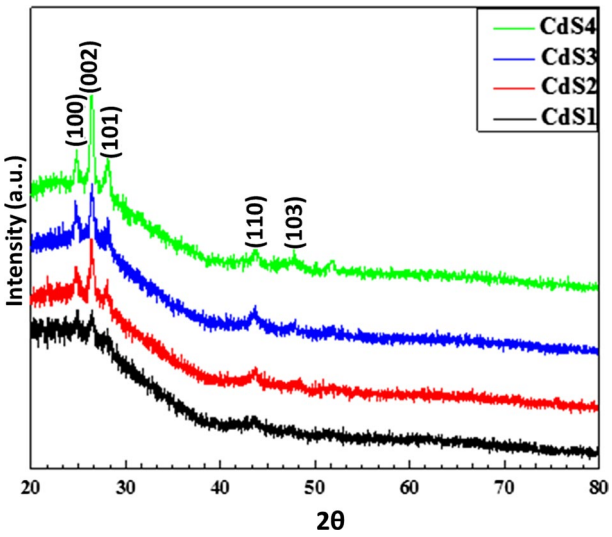


**Fig. 4** XRD pattern of CdS**1**, CdS**2**, CdS**3** and CdS**4** thin films

that result in further development of the crystal structure of CdS**4** thin film. Main grain sizes of CdS**1**, CdS**2**, CdS**3** and CdS**4** thin films were calculated to be 8.55 nm, 10.85 nm, 11.92 nm and 15.01 nm, respectively. The thickness of CdS thin film increases, as grain size constituting thin film also slightly increases (Tsai et al. 1996) and this can increase the mobility and transfer charge carriers in CdS thin films (Ikhmayies and Ahmad-Bitar 2008; Zahra 2013).

### 3.2 Morphological analysis

Mean size of particles composing CZTS**4** thin film was found between 300 and 500 nm as seen in SEM and AFM images given in Fig. 5a, b. This size is not very large compared to that annealed at 375 °C temperature, but it can be accepted to be large enough to provide a path for minority charge carriers transported to depletion region (Riha 2011). Also, CZTS**4** thin film consists of dense particles with an inhomogeneous size distribution. The thickness of CZTS**4** thin film is about 700 nm. The roughness value for CZTS**4** thin film was measured to be about 60 nm and this value is somewhat higher compared to that obtained for annealed films. it can be said that this roughness can cause a leakage current in CdS/CZTS heterojunction diode (Sun et al. 2017).

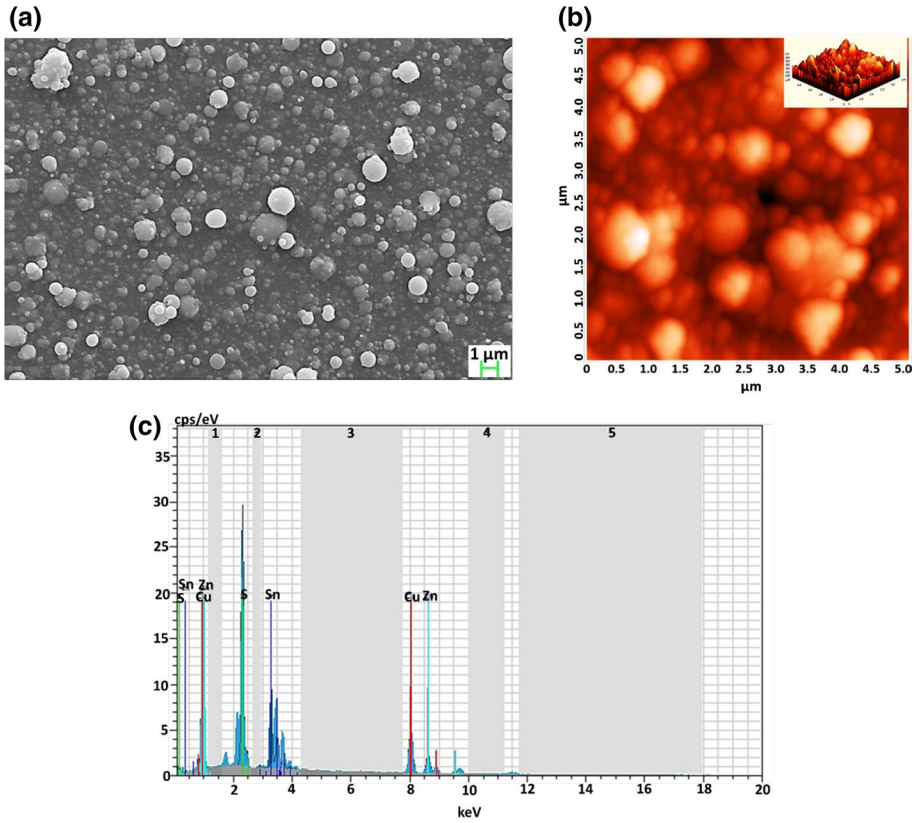


**Fig. 5** **a** SEM and **b** AFM (5 µm × 5 µm area) images, and **c** SEM–EDX Spectrum of CZTS4 thin film

**Table 1** The atomic ratios of the elements in CZTS**4** thin film

| Cu (%) | Zn (%) | Sn (%) | S (%) | Cu/(Zn + Sn) | S/metal |
|---|---|---|---|---|---|
| 27.85 | 12.93 | 13.29 | 45.93 | 1.06 | 0.84 |

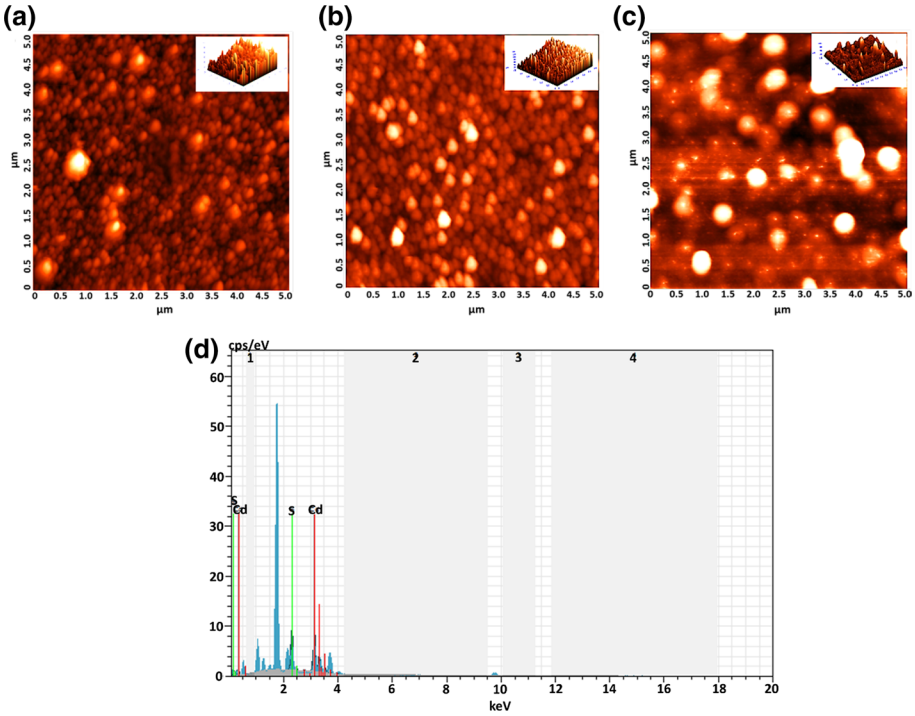


**Fig. 6** AFM images are given in **a)** for CdS**1**, in **b** for CdS**2** thin films, **c** for CdS**4** thin films (5 μm × 5 μm area) and **d** SEM–EDX spectrum of CdS**2** thin film

Atomic ratios of elements in CZTS**4** thin film are expressed in Table 1. and SEM–EDX spectrum is given in Fig. 5c. CZTS**4** thin film is slightly Cu-rich and Zn-poor. Therefore, defects in $Cu_{Zn}$ antisite, $Cu_{Sn}$ antisite and $Sn_{Zn}$ antisite can occurs in CZTS**4** thin film (Yeh et al. 2016; Yin et al. 2015). These defects can play role as trap to charge carriers within CZTS thin film, leads to life time of minority charge carriers to be shorter (Courel et al. 2016), and this situation adversely affect efficiency of diodes. However, the stoichiometry of CZTS**4** thin film produced has not shown any significant compositional deviation.

The particles forming CdS**1** thin film consist of small size and inhomogeneous size distribution, according to AFM image given in Fig. 6a. CdS**1** thin film was produced in a short time and since number of particles reached at substrate was quite low, the number of particles formed CdS**1** thin film was limited. Therefore, the particles forming CdS**1** thin film produced were obtained to be in small grain sizes (Gezgin et al. 2017). This can lead to formation of pinholes, low shunt resistivity and thus formation of a leakage current in solar cells (Tashkandi and Sampath 2011). However, particles forming CdS**2** thin film have a larger and more homogeneous size distribution. CdS**2** thin film was deposited for a longer time duration. CdS particles are ablated during deposition process which come on CdS particles on substrate and cause particle growth (Gezgin et al. 2017). Thus, size of particles forming CdS**2** thin film is

**Table 2** The atomic ratios of the elements in CdS2 thin film

| Cd (%) | S (%) | Cd/S |
|---|---|---|
| 49.99 | 50.01 | 0.99 |

greater than particle size of that in CdS**1** thin film. Figure 6c shows AFM image of CdS**4** thin film annealed at 200 °C temperature. The size of the particles forming the CdS**4** thin film is greater than that of in CdS**1** and CdS**2** thin films. Due to the effect of the annealing temperature, the moving particles combined with each other to form larger particles in CdS**4** thin film.

The ratio of atomic elements in CdS**2** thin film was determined by a SEM–EDX spectrum given in Fig. 6d and listed in Table 2. The ratio of atomic elements in [Cd]/[S] = 0.99 (Islam et al. 2013; Manikandan et al. 2015), which confirms the stoichiometric formation of CdS thin film. So, the stoichiometric structure of CdS target material processed by PLD was quite well transferred to CdS thin film structure.

### 3.3 Optical properties of thin films

CZTS**4** thin film has a high absorption rate according to absorption spectrum given in Fig. 7a. Band gap of CZTS**4** thin film is expressed by the following Tauc law:

$$(\alpha h\nu)^2 = A\left(h\nu - E_g\right)^{1/2} \tag{2}$$

Here, A is a constant, $E_g$ is the band gap of thin film, is acquired by extrapolation of linear line of $(\alpha h\nu)^2$ versus $(h\nu)$ in Tauc plot as shown in Fig. 7b, $h\nu$ is the photon energy (Bedia et al. 2013; Keskenler et al. 2013). The band gap of CZTS thin film was calculated to be about 1.47 eV (Xinkun et al. 2012). The typical band gap of CZTS thin film is about 1.5 eV (Malerba et al. 2014; Vanalakar et al. 2014). The band gap of CZTS**4** thin film is somewhat lower than this range given in literature. The elemental ratio of [Cu]/[Zn] + [Sn] = 1.06 demonstrates that CZTS**4** thin film is rich in copper and, the donor deep levels in the band of CZTS thin film cause some lower band gap (Aizawa et al. 2013; Yeh et al. 2016).

CdS**2** thin film among four of CdS (**1**,**2**,**3, 4**) thin films has an ideal absorption spectrum as n-type buffer layer according to absorption spectra given in Fig. 8a. CdS**2** thin film transmits quite high amount of photons in the visible region, but absorbs a small amount of photons in the infrared region (Ortuño-López et al. 2013). In particular, photon conduction of CdS**2** and the photon absorption of CZTS thin film in the visible region allow photo-induced charge carriers to be formed. CdS**4** thin film absorbs photon in visible region in contrast to CdS**2** thin film that may be due to the fact that CdS**4** thin film is composed of larger particles. The photons absorbed in the visible region by CdS**4** thin film cannot be transmitted to the absorber layer that causes the photo-current and $J_{sc}$ value of the diode to decrease. Band gaps of CdS**1**, CdS**2**, CdS**3** and CdS**4** thin films have been calculated to be 2.42 eV, 2.40 eV, 2.40 eV and 2.36 eV, respectively, according to Tauc plot in Fig. 8b. Band gaps of these three thin films provide compatibility with the literature (Oliva et al. 2001; Rupali et al. 2018).

### 3.4 Electrical properties of ITO/CZTS/CdS/Ag, ITO/CdS/CZTS/Ag and ITO/CdS(annealed)/CZTS/Ag diodes

J–V characteristics of CdS thin films are given depending on thickness of thin films under a dark and illumination conditions in Fig. 9a, b, respectively. Their resistivity decreases

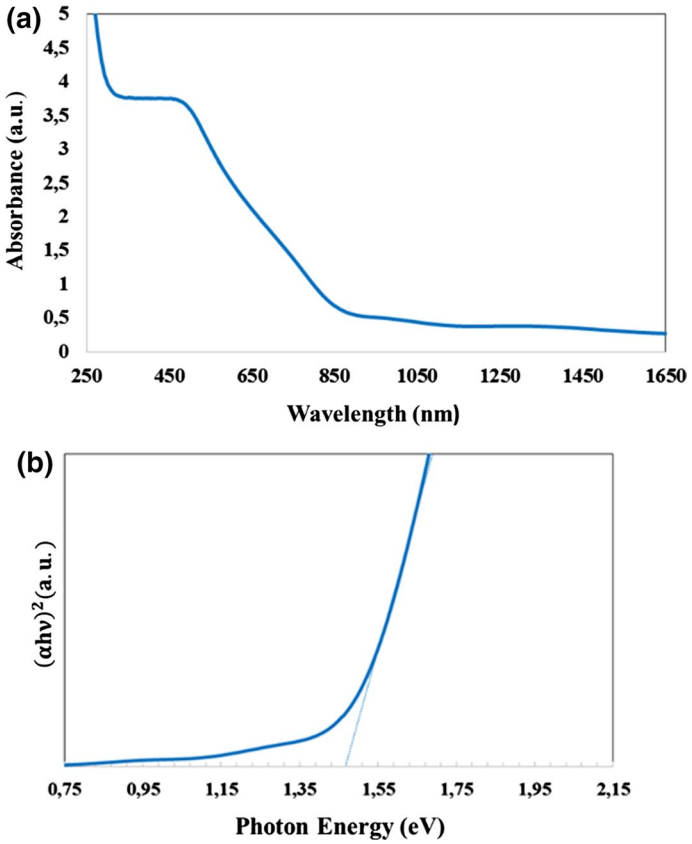


**Fig. 7** **a** The absorbance spectrum and **b** Tauc Plot of CZTS**4** thin film

while thickness of thin films increases in dark environment as shown in Fig. 9a. Namely, the grain size of thin film increases as thickness of CdS thin films increases. As grain boundary numbers decrease while the size of graind increase, traps and defects in grain boundaries are passivized. In addition, the crystalline property of CdS thin film increases and the charge carriers move freely in thin film without being destroyed by the traps. Thus, the resistivity of CdS thin films reduce (Enríquez and Mathew 2003; Kathirvel et al. 2011; Moreno-Regino et al. 2019). Also, the lifetime of charge carriers increases as traps reduce. However, since the crystal structures of CdS**2** and CdS**3** thin films are very close to each other, resistances are very close to each other. The photocurrent of CdS thin films slightly increase under illumination conditions according to J–V graph in Fig. 9b. The electrons in the valence band of thin films were transferred to conduction band and, increase photoconductivity by forming free charge carriers (Aruna-Devi et al. 2019; Das et al. 2019; Henry et al. 2016). Some increase in thickness of CdS thin film results in more photo-excited charge carriers, better charge transitions and more photo-current under illumination. This is based on a higher photon absorption of thin film and the improvement of the crystal structure, as stated above.

J–V curve and J–V logarithmic curve of CZTS-I, CZTS-II and CZTS-III diode structures in dark conditions are demonstrated in Fig. 10a, b. Diodes show the rectification

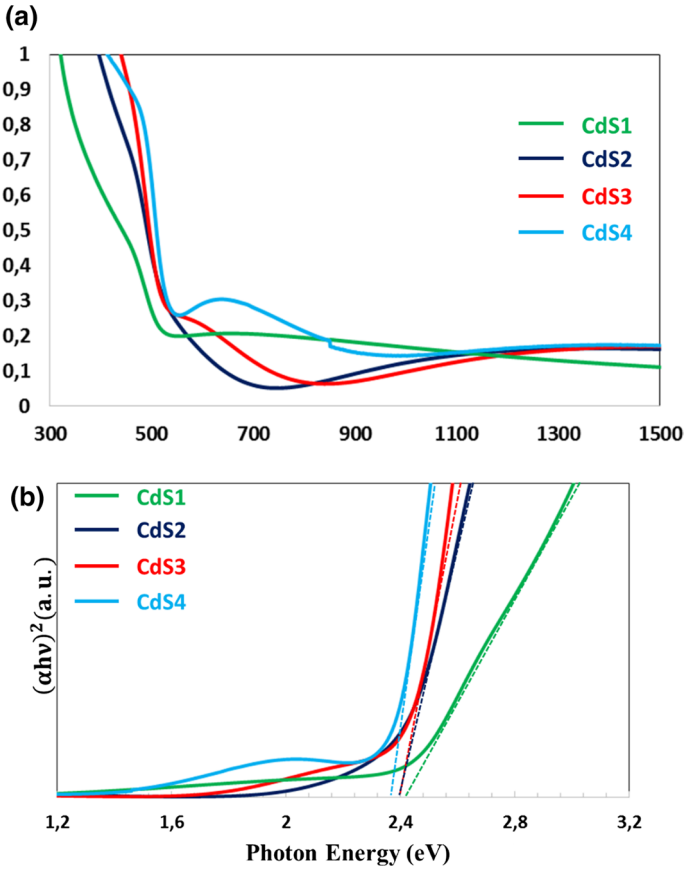


**Fig. 8** **a** The absorption spectrum and **b** Tauc Plot of CdS**1**, CdS**2,** CdS**3** and CdS**4** thin films

behaviour. CZTS**4**, CdS**2** and CdS**4** thin films, are close to stoichiometric and polycrystalline structure, behave like p- and n-type semiconductors causing the diode to perform rectification behaviour (Boutebakh et al. 2017; Saha et al. 2017). Furthermore, CZTS**4** thin film with 1.47 eV band gap provides relatively compatible band gap alignment with CdS (**2**,**4**) thin films (with the band gaps of 2.40 eV and 2.36 eV) (Crovetto and Hansen 2017) which leads to built-in potential and appropriate charge transfer between semiconductors and provide rectification (Htay et al. 2011).

The thermionic emission theory is used to define the exhibition of rectification behaviour for CZTS-I, CZTS-II and CZTS-III diode. According to theory, the current is defined by Eq. (3),

$$I = I_o\left[\exp\left(qV/nkT\right) - 1\right] \tag{3}$$

where $I_o$ is the saturation current, $k$ is Boltzmann constant, $q$ is the elementary electric charge, $V$ is applied voltage, T is the absolute temperature and $n$ is the ideality factor.

The ideality factor $n$ is given as

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \tag{4}$$

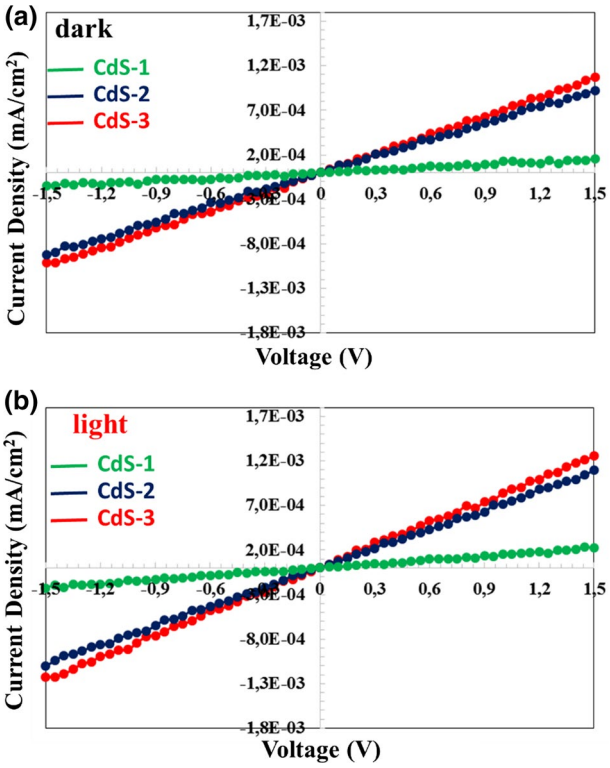


**Fig. 9** J–V characterisations of CdS**1**, CdS**2** and CdS**3** thin films in the **a** dark and **b** under the illumination

The ideality factor is calculated from the slope (m) of the straight part of semi-logarithmic curve of the forward bias J–V characteristic. The slope $m_1, m_2$ and $m_3$ have been calculated to be 1.3, 1.6 and 1.5 from the forward bias of log J- log V semi logarithmic characteristics of CZTS-I, CZTS-II and CZTS-III diode structures depicted in Fig. 10b, respectively. The ideality factors of $n_1, n_2$ and $n_3$ of CZTS-I, CZTS-II and CZTS-III diode structures have been calculated to be 4.64, 3.86 and 3.48, respectively, by using Eq. (4). The best rectification behaviour was achieved by CZTS-III diode. This can be attributed to that the better p–n junction can be established due to the better crystal structure and more ideal surface hardness of CZTS**4** thin film and thus, the leakage current is lower due to the low number of defects in p-n interface.

However, the ideality factor for an ideal diode structure must be within $1 < n < 2$ interval (Patel et al. 2013), but it has been found and interpreted in the present work that all diode structures have ideality factors greater than this range (Boutebakh et al. 2017). Higher ideality factor are based on several reasons. If the case is that, pinholes and cracks may have formed in CZTS**4** thin film due to annealing at 375 °C sulfurization temperature (Feng et al. 2017; Mkawi et al. 2014). In addition, pinholes can be also formed in CdS**2** thin film since it may not have enough thickness. These pinholes cause low shunt resistance in the diode structure resulting in a leakage current (Liao et al. 2018; Servaites et al. 2011). This situation causes a large ideality factor of the diodes (Gopal et al. 2015; Liao et al. 2018; Servaites et al. 2011).

For a metal contact to exhibit ohmic behavior for p-type semiconductor, work function of metal ($\Phi_M$) must be greater than work function of ($\Phi_S$) the semiconductor

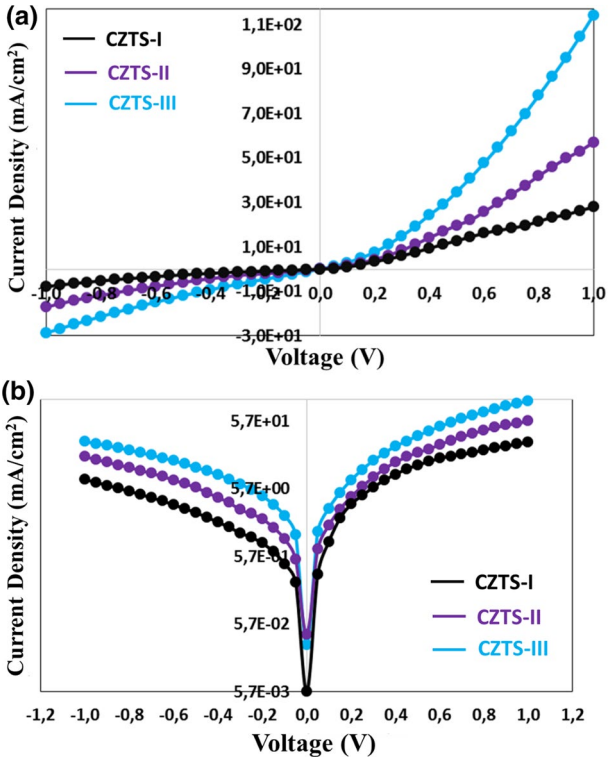


**Fig. 10** **a** J–V curve and **b** J–V logarithmic curve for CZTS-I, CZTS-II and CZTS-III diode structures in dark conditions

$(\Phi_M > \Phi_S)$(Boutebakh et al. 2017). But, Ag back contact exhibits relatively non ohmic behaviour for ITO/CdS/CZTS/Ag diode structure. Namely, work function of Ag metal (4.6 eV) (Cheggstudy 2019) is lower than work function of CZTS thin film (5.5 eV). There is no ideal band alignment between Ag metal and CZTS semiconductor, and Ag metal forms a high barrier height for CZTS semiconductor and exhibits schottky contact behaviour (Boutebakh et al. 2017). Ag metal thin film cannot exhibit a regular ohmic behaviour for CZTS thin film leading a high contact resistivity (Boutebakh et al. 2017; Long et al. 2018). Therefore, it is prevented that the transition of photo-excited holes in CZTS thin film to Ag metal contact and charge collection can be limited. In order to overcome this problem, Nickel (Ni), Cobalt (Co), Palladium (Pd) and Gold (Au) metals with higher work functions (Ayalew 2019) can be used as ohmic contact for p-type CZTS semiconductor (Boutebakh et al. 2017; Long et al. 2018; Sarswat and Free 2013). Thus, the barrier height between the semiconductor and these metals is reduced and these metals can exhibit a behaviour close to the ohmic contact for hole transition from p-type CZTS (Aftab et al. 2019; Li et al. 2017). Furthermore, since work function of ITO layer (5.25 eV) is larger than work function of n-type CdS semiconductor (4.7 eV), contact resistance is high (Chen et al. 2018). These situations lead to high serial resistance, different barrier heights and thus high idealty factors for CZTS-II and CZTS-III devices (Boutebakh et al. 2017). In addition, CZTS-III diode structure among the three diodes has the lowest ideality factor. But, ideality factor of CZTS-III diode is still a little high. Although CdS**4** thin film has a better crystalline structure than other CdS thin

films, pinholes and cracks may be formed in CdS**4** thin film due to the annealing temperature which results in high idealtiy factor.

Work function of ITO layer should be higher than work function of CZTS thin film for ITO layer to display ohmic behaviour to p-type CZTS semiconductor thin film (Gupta and Dixit 2018; Kurhade 2015; Rhoderick 1982). If work function of ITO layer is high, the barrier height falls between that of ITO layer and p-type CZTS thin film. Thus, the hole charge carriers in CZTS are collected at rear contact and therefore, electron charge carriers are collected at deplation region. However, in this respect, ITO with 5.25 eV work function cannot show a good ohmic behaviour for CZTS thin film with 5.5 eV work function (Kim et al. 2016; Patel et al. 2013; Saha and Alam 2018; Tao et al. 2014). ITO has a resistance higher than that of metal contacts (Mo and Au). This situation effects ohmic behaviour negatively (Bouchama and Ali-Saoucha 2017; Espindola-Rodriguez et al. 2017; Ge et al. 2014; Kim et al. 2016; Myny et al. 2016). Furthermore, while CZTS thin film is annealed at 375° sulfurization temperature, the electrical conductivity of ITO layer decreases and series resistance of the diode increases (Ge et al. 2014; Kim et al. 2016). The ideality factor of CZTS-I diode structure is high under these conditions.

CdS thin film was not exposed to any annealing after it was deposited on a coated ITO glass at room temperature. Therefore, although CdS thin film is in crystal structure, it cannot be hardened ideally (Wang et al. 2011). In addition, CZTS thin film was grown on CdS thin film and annealed at 375 °C sulfurization temperature. Thus, It is highly possible to embedded CZTS thin film into ideally non-hardened CdS**2** thin film throughout sulfurization annealing process. This adversely effects the building of depletion region resulting in some defects in depletion region (Tanaka et al. 2009; Yan 2016b). Thus, CZTS-II diode structure shows some higher ideality factors. Furthermore, as expressed for CZTS-I diode structure, pinholes and cracks possibly occurring in CZTS**4** and CdS**2** thin films causes some leakage current and low shunt resistance in CZTS-II diode structure, too (Cantas et al. 2018; Tashkandi 2012). This morphological formation also causes high ideality factor of CZTS-II diode.

J–V characteristics of CZTS-I, CZTS-II and CZTS-III diodes under the illumination condition (AM 1.5 solar radiation of 80 mW/cm$^2$) are given in Fig. 11. All CZTS diodes exhibit photo-electric behaviour under the illumination condition. CdS and CZTS thin films are crystal structure and their stoichiometric structures are very close to what is desired. Also, band gaps of CdS (2.36 and 2.4 eV) and CZTS (1.47 eV) thin films ensures a compatible band alignment with each other (Crovetto and Hansen 2017; Htay et al. 2011). These circumstances can lead to formation of a p-n heterojunction, which

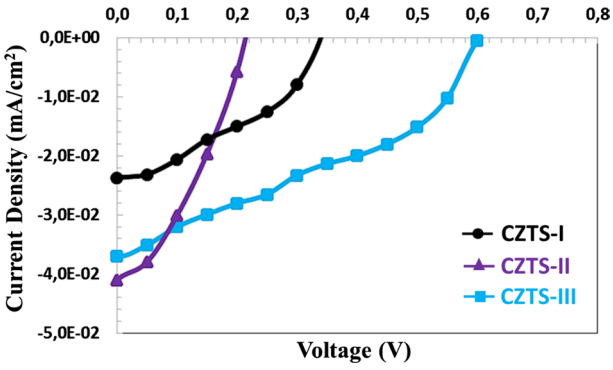


**Fig. 11** J–V plot of CZTS-I, CZTS-II and CZTS-III diode structures under illumination conditions

ensure formation of photo-excited charge carriers in an absorber layer when photon enters into CZTS. Thus, the diode generates photo current. Table 3 shows some electrical parameters of CZTS-I, CZTS-II and CZTS-III diodes.

$J_{sc}$, $V_{oc}$, FF and η values of CZTS-I diode are determined to be 0.024 mA/cm$^2$, 350 mV, 0.30 and 0.0030%, respectively. $J_{sc}$ of the diode is found to be very low. This situation can be based on following reasons: Since light irradiates directly CZTS thin film (so, diffuse from ITO layer to CZTS layer), it can be absorbed immediately near ITO contact without diffusing much into CZTS thin film. The most of photo excited charge carriers can undergo recombination before they reach space charge region (SCR). A low amount of photo excited charge carriers is formed in a region near the depletion region since a small amount of light can reach into the depletion region. Also, since some photo excited electron charge carrier are close to ITO layer, they prefer to go to ITO contact instead of SCR. This reduces the photo current and hence the short-circuit current density (Bouchama and Ali-Saoucha 2017; Espindola-Rodriguez et al. 2017; Ge et al. 2014; Kim et al. 2016; Myny et al. 2016).

Since the produced CZTS**4** thin film is Cu rich, $Cu_{Zn}$ antisite, $Cu_{Sn}$ antisite and $Sn_{Zn}$ antisite defects can be composed in CZTS structure. These defects act as a recombination point to photo-excited charge carriers and, therefore, it reduces life time of minority charge carriers and charge collection in depletion region (Breitenstein et al. 2010; Gezgin et al. 2017; Gordillo et al. 2018; Yeh et al. 2016; Yin et al. 2015). In addition, CZTS thin film is crystalline, but not composed of very large particles. This situation indicates that number of grain boundaries is slightly higher. Traps positioned within these grain boundaries act as a recombination centre (Gaury and Haney 2016; Harder et al. 2005) for charge carriers, inhibit the transfer of electron charge carriers to the side of depletion region which is one of reasons why $J_{sc}$ value is low (Ishibashi et al. 2017; Suzuki et al. 2014; Tubtimtae et al. 2014; Yang et al. 2015).

Even if CdS thin film has been deposited on CZTS thin film with low laser pulse energies, CdS particles ablated from CdS target can be diffused into CZTS thin films (Yan 2016a) and may form some defects and trap points in depletion region and CZTS thin film (Tanaka et al. 2009). Also, roughness value of CZTS thin film due to annealing leads to some trap formation in depilation region and adversely effects formation of depletion region. Therefore, charge carriers are recombined in depletion region which limits collection of charges, and $J_{sc}$ value remains low (PVeducation 2019; Tanaka et al. 2009). In addition, although CdS**2** thin film has polycrystalline structure, its grain size is slight small. The number of grain boundaries in film is high and traps are located within these boundaries. Therefore, charge transfer within CdS**2** thin film may be prevented and electrical resistance of CdS**2** thin film may be high (Oztas 2018) resulting in a low charge collection and low $J_{sc}$ value (Sugano et al. 2017).

The open circuit voltage is not as low as $J_{sc}$, but not high. The low $V_{oc}$ value can be based on a low band gap of CZTS thin film. Low band gap causes $V_{oc}$ value to drop $\left(\frac{E_g}{q} - V_{oc}\right)$. Because, $V_{oc}$ value is directly proportional to distinction between quasi-Fermi

**Table 3** Electrical parameters determined of CZTS-I, CZTS-II and CZTS-III diode structures

| Sample diode | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | η (%) |
|---|---|---|---|---|
| CZTS-I | 0.024 | 350 | 0.30 | 0.0030 |
| CZTS-II | 0.040 | 220 | 0.37 | 0.0038 |
| CZTS-III | 0.037 | 600 | 0.36 | 0.01 |

levels of n-type and p-type semiconductors forming p-n heterojunction (Bourdais et al. 2016; Polizzotti et al. 2013; Qi and Wang 2012; Tayagaki et al. 2013; Yan et al. 2015).

Cracks and pinholes generated in CZTS and CdS thin films as discussed in details which cause a leakage current in the diode and therefore shunt resistance of device is low (Cantas et al. 2018; Tashkandi 2012). This situation and some relevant reasons causing CZTS-I and CZTS-II diode structures to have a large ideality factor leading both low $V_{oc}$ and $J_{sc}$ values of both CZTS-I and CZTS-II diodes (Breitenstein et al. 2010; Nath et al. 2011; Pveducation.org 2019). Also, ITO contact cannot exhibit a good ohmic behaviour for CZTS thin film causing a low $J_{sc}$, $V_{oc}$ and η values of CZTS-I diode.

$J_{sc}$, $V_{oc}$, FF and η values of CZTS-II diode were determined to be 0.040 mA/cm$^2$, 220 mV, 0.37 and 0.0038%, respectively. $J_{sc}$ value for diode is low, but higher than $J_{sc}$ value of CZTS-I diode. However, incident light comes directly from ITO layer to CdS**2** thin film and diffuses into CZTS thin film without considerable absorption in CdS**2** thin film. Thus, light generates more photo-excited charge carriers in CZTS**4** thin film without too much loss in path as it is in CZTS-I diode (Bouchama and Ali-Saoucha 2017; Espindola-Rodriguez et al. 2017; Ge et al. 2014; Kim et al. 2016; Myny et al. 2016). The most of electron charge carriers produced are not recombined in rear contact and transferred to SCR. As a result, $J_{sc}$ value of CZTS-II diode structure is higher than $J_{sc}$ value of CZTS-I diode structure. In addition, an increase in short circuit current density causes an increase in fill factor.

The value of $V_{oc}$ of CZTS-II diode decreases compared to that of other diodes. It has been stated above that depletion region in p-n heterojunction is likely to deteriorate due to the annealing of CZTS**4** thin film in 375 °C sulfurization temperature. Defect formation in depletion region at p-n interface can lead to recombination of charge transitions, irregular charge collection and leakage current (Chakrabarti et al. 2006). This situation can cause $V_{oc}$ value to be low (Bhattacharya et al. 1986; Nath et al. 2011). In addition, as stated above, the fact that Ag and ITO contacts on CZTS-II diode cannot exhibit ideal ohmic behaviour which causes low $J_{sc}$ and $V_{oc}$ values.

$J_{sc}$, $V_{oc}$, FF and η values of CZTS-III diode are measurement to be 0.037 mA/cm$^2$, 600 mV, 0.36 and 0.01%, respectively. The process of formation of CZTS-II and CZTS-III diodes is the same, but only difference is that CdS thin film has been annealed at 200 °C temperature in CZTS-III diode. Because CdS**4** thin film has been annealed, its crystal structure has improved and the size of particles forming this thin film has increased. CdS**4** thin film absorbed more photons in the visible region due to larger particle size. The transition of visible region photons into CZTS thin film has been restricted and photocurrent in CZTS-III diode has been reduced. The number of photo-excited charge carriers in CZTS thin film was decreased and $J_{sc}$ value of CZTS-III diode was also decreased compared to CZTS-II diode. Furthermore, the surface hardness of CdS**4** thin film is likely to increase due to the annealing at 200 °C temperature (Blum et al. 1999; Chang et al. 2010; Fernández-Pérez and Sandoval-Paz 2016; Wang et al. 2011, 2019). The diffusion of CZTS atoms into CdS**4** thin film is prevented during the deposition and annealing of CZTS thin film (Kariper 2016). The number of defects and traps are reduced in depletion region because the number of impurities there are small. Thus, recombination centres in the depletion region are reduced, more charges are collected at the edge of the depletion region and higher built-in voltage is established in p–n junction (Kanevce et al. 2017). This situation increases $V_{oc}$ value of CZTS-III diode (Kanevce et al. 2017). In addition, annealing of CdS thin film reduces the barrier height between the ITO contact and CdS thin film. The annealing of the CdS**4** thin film also reduces the electrical resistance of CdS**4** thin film. Thus, reducing in series resistance can cause $V_{oc}$ to increase (Mahala et al. 2015; Thibert et al. 2013). The fact that the CdS**4** thin film consists of a larger grain size results

in reduction in the grain boundary number. Thus, the defects between the grain boundaries are passivized, its crystal structure is improved, the recombination rates of charge carriers are reduced and thus, $V_{oc}$ value increases.

An increase in $J_{sc}$ and FF values of CZTS-II and CZTS-III diodes enhances η value compared to that of CZTS-I diode. In CZTS-II and CZTS-III diodes, the incident light comes directly from ITO layer into a buffer layer (CdS) instead of an absorber layer (CZTS). Thus, more photo-exited charge carriers occur in the depletion region and in the site close to the depletion region (in CZTS absorber layer). This increases $J_{sc}$ and therefore η values. However, CZTS diode structures exhibit photo-electric behaviour when light comes from ITO layer to both CZTS and CdS layers. If both sides of these diodes are illuminated, the diodes can act as diodes in bifacial solar cells, the high number of photo-excited charge carriers are formed in the diode and thus, $J_{sc}$, and η values of the diodes can increase more.

Some steps must be performed in order to ensure high $J_{sc}$, $V_{oc}$ and η values of diodes: ***i***- CZTS thin film must be annealed at a suitable sulfurization temperature in order to reduce number of grain boundaries and avoid pinholes and cracks. ***ii***- High resistance transparent oxide window (i-ZnO) layer can be used to prevent leakage current. ***iii***- When CZTS and CdS thin films are deposited, in order to slow down particles that are ablated from target (CdS and CZTS target materials) and to prevent them from diffusing into thin films (CdS and CZTS thin films) on ITO glass, an ambient inert gas (as Ar) should be used at an appropriate pressure in vacuum chamber.

## 4 Conclusıons

In this work, ITO/CZTS/CdS/Ag and ITO/CdS/CZTS/Ag heterojunction diodes have been produced. CdS and CZTS layers have been produced on ITO glass at room temperature by PLD technique. CZTS was grown in amorphous structure at room temperature and then annealed at several sulfurization temperatures in 325 °C, 350 °C and 375 °C, and then, was transformed into polycrystalline structure for each annealing temperature. It has been observed that CZTS**4** thin film, after annealing at 375° temperature, has denser crystal peaks and a larger grain sizes. CdS thin films were deposited on a substrate at room temperature for 10, 15 and 20 min and, also, CdS thin film produced in 20 min was annealed at 200 °C temperature. All CdS thin films have polycrystal structure. CdS**1** thin film shows some weaker crystal peaks whereas CdS**2** and CdS**3** exhibit more intense crystal peaks. CdS**4** thin film has better crystal structure than all CdS thin films. CdS**2** and CdS**4** thin films were used as a buffer layer in diode structures.

Ideality factor of CZTS-I heterojunction diode in dark condition was calculated to be 4.64. In addition, the diode have shown a photo-electric property in illumination conditions. $J_{sc}$, $V_{oc}$, FF and η values for CZTS-I diode under illumination conditions were determined to be 0.024 mA/cm$^2$, 350 mV, 0.30 and 0.003%, respectively. The ideality factor of CZTS-II diode has been calculated to be 3.86. The diode has exhibited a photo-electric behaviour in illumination conditions and has $J_{sc}$, FF, $V_{oc}$ and η values which were measurement to be 0.040 mA/cm$^2$, 220 mV, 0.37 and 0.0038%, respectively. $J_{sc}$ values of both devices are low. CZTS-III diode' ideality factor has been determined as 3. 48, its $J_{sc}$, FF, $V_{oc}$ and η values are 0.037 mA/cm$^2$, 600 mV, 0.36 and 0.01%, respectively.

CZTS-I, CZTS-II and CZTS-III diode structures exhibit photo-electric behaviour when light comes from ITO layer to both CZTS (CZTS-I) and CdS layers (CZTS-II and CZTS-III). This shows that if both sides of devices produced in this work are illuminated, they

can act as diodes in bifacial solar cells and thus, $J_{sc}$, $V_{oc}$, FF and η values of these diodes can be increased.

**Acknowledgements** Authors kindly would like to thank: Scientific and Technical Research Council of Turkey (TUBITAK) for financial support via Grant No. 1649B031503748; Selçuk University, High Technology Research and Application Center for supplying with Infrastructure; Selçuk University Scientific Project Coordination office for grands via projects with references of 18401124 and 15201070.

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